ICM-42607-P Datasheet

Premium Performance 6-Axis MotionTracking™ IMU

ICM-42607-P HIGHLIGHTS

The ICM-42607-P is a 6-axis MEMS MotionTracking device that combines a 3-axis gyroscope and a 3-axis accelerometer. It has a configurable host interface that supports I3C℠, I²C and SPI serial communication, features up to 2.25 Kbytes FIFO and 2 programmable interrupts with ultra-low-power wake-on-motion support to minimize system power consumption.

The ICM-42607-P supports the lowest gyro and accel sensor noise in this IMU class, and has the highest stability against temperature, shock (up to 20,000g) or SMT/bend induced offset as well as immunity against out-of-band vibration induced noise.

Other industry-leading features include on-chip APEX Motion Processing engine for gesture recognition, activity classification, and pedometer, along with programmable digital filters, and an embedded temperature sensor.

The device supports a VDD operating range of 1.71V to 3.6V, and a separate VDDIO operating range from 1.71V to 3.6V.

ICM-42607-P FEATURES

- Gyroscope Noise: 8 mdps/√Hz & Accelerometer Noise: 110 µg/√Hz
- Low-Noise mode 6-axis current consumption of 0.55 mA
- Low-Power mode support for always-on experience
- User selectable Gyro Full-scale range (dps): ± 250/500/1000/2000
- User selectable Accelerometer Full-scale range (g): ± 2/4/8/16
- User-programmable digital filters for gyro, accel, and temp sensor
- APEX Motion Functions: Pedometer, Tilt Detection, Wake on Motion, Free-Fall Detection, Significant Motion Detection
- Host interface: 12.5MHz I3C℠, 1MHz I²C, 24MHz SPI

APPLICATIONS

- Smartphones, Computers, Tablets
- Smart Watches and Fitness Trackers
- Augmented & Virtual Reality Headsets and Controllers
- Game Controllers
- IoT Applications
- Drones and Robotics

BLOCK DIAGRAM

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICM-42607-P†	–40°C to +85°C	2.5x3mm 14-Pin LGA

†Denotes RoHS and Green-Compliant Package

TDK-INVENSENSE SENSORS FOR SMARTPHONE, MOBILE & IOT APPLICATIONS

Parameter	ICM-42607-P Sensorhub	ICM-42605 Sensorhub	ICM-42686-P Handheld Action	ICM-42688-P HMD & Robotics
GYRO Noise (mdps/rt-Hz)	8	3.8	5.3	2.8
GYRO Offset Temp Stability (mdps/°C)	±30	±20	±10	±5
GYRO Range & Resolution	±2000dps; 16-bits	±2000dps; 16-bits	±4000dps; 16/19-bits	±2000dps; 16/19-bits
ACCEL Noise (µg/rt-Hz)	110	70	70	AXY: 65; AZ: 70
ACCEL Range & Resolution	±16g; 16-bits	±16g; 16-bits	±32g; 16/18-bits	±16g; 16/18-bits
ODR & Sample Synch	1.6kHz; No RTC	8kHz; No RTC	32kHz; RTC	32kHz; RTC

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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-42607-P Single-Interface MotionTracking device. The device is housed in a small 2.5x3x0.76 mm 14-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-42607-P is a 6-axis MotionTracking device that combines a 3-axis gyroscope and a 3-axis accelerometer in a small 2.5x3x0.76 mm (14-pin LGA) package. It also features up to 2.25 Kbytes FIFO that can lower the traffic on the serial bus interface and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-42607-P, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope supports four programmable full-scale range settings from ±250dps to ±2000dps and the accelerometer supports four programmable full-scale range settings from ±2g to ±16g.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I3C^{SM}, I^{2}C and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate VDDIO operating range of 1.71V to 3.6V.

The host interface can be configured to support I3C^{SM} slave, I^{2}C slave, or SPI slave modes. The I3C^{SM} interface supports speeds up to 12.5MHz (data rates up to 12.5Mbps in SDR mode, 25Mbps in DDR mode), the I^{2}C interface supports speeds up to 1MHz, and the SPI interface supports speeds up to 24MHz.

The device provides high robustness by supporting 20,000*g* shock reliability.

1.3 APPLICATIONS

- Smartphones, Computers, Tablets
- Smart Watches and Fitness Trackers
- Augmented & Virtual Reality Headsets and Controllers
- Game Controllers
- IoT Applications
- Drones and Robotics

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-42607-P includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with programmable full-scale range of ±250, ±500, ±1000, and ±2000 degrees/sec
- Low Noise (LN) power mode support
- Digitally programmable low-pass filters
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-42607-P includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with programmable full-scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g*
- Low Noise (LN) and Low Power (LP) power modes support
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 MOTION FEATURES

ICM-42607-P includes the following motion features, also known as APEX (**A**dvanced **P**edometer and **E**vent Detection – ne**X**t gen)

- Pedometer: Tracks Step Count, also issues Step Detect interrupt
- Tilt Detection: Issues an interrupt when the Tilt angle exceeds 35° for more than a programmable time
- Free-Fall Detection: Issues an interrupt when free-fall is detected
- Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold
- Significant Motion Detection: Detects Significant Motion if Wake on Motion events are detected during a programmable time window

2.4 ADDITIONAL FEATURES

ICM-42607-P includes the following additional features:

- Up to 2.25 Kbytes FIFO buffer enables the applications processor to read the data in bursts
- User-programmable digital filters for gyroscope, accelerometer, and temperature sensor
- 12.5MHz I3C^{SM} (data rates up to 12.5Mbps in SDR mode, 25Mbps in DDR mode) / 1 MHz I^2C / 24 MHz SPI slave host interface
- Digital-output temperature sensor
- Smallest and thinnest LGA package for portable devices: 2.5x3x0.76 mm (14-pin LGA)
- 20,000 *g* shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Conditions, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	GYRO_UI_FS_SEL=0		±2000		º/s	2
	GYRO_UI_FS_SEL=1		±1000		º/s	2
	GYRO_UI_FS_SEL=2		±500		º/s	2
	GYRO_UI_FS_SEL=3		±250		º/s	2
Gyroscope ADC Word Length	Output in two's complement format		16		bits	2
Sensitivity Scale Factor	GYRO_UI_FS_SEL=0		16.4		LSB/(º/s)	2
	GYRO_UI_FS_SEL=1		32.8		LSB/(º/s)	2
	GYRO_UI_FS_SEL=2		65.5		LSB/(º/s)	2
	GYRO_UI_FS_SEL=3		131		LSB/(º/s)	2
Sensitivity Scale Factor Initial Tolerance	Component & Board-level, 25°C		±1		%	1
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±0.01		%/ºC	3
Nonlinearity	Best fit straight line; 25°C		±0.2		%	3
Cross-Axis Sensitivity	Board-level		±2		%	3
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	Board-level, 25°C		±1		º/s	3
ZRO Variation vs. Temperature	-40°C to +85°C		±0.015		º/s/ºC	3
OTHER PARAMETERS						
Rate Noise Spectral Density	@ 10 Hz		0.008		º/s /√Hz	3
Total RMS Noise	Bandwidth = 100 Hz		0.08		º/s-rms	4
Gyroscope Mechanical Frequencies		24.69		30.49	kHz	1
Low Pass Filter Response	ODR < 1kHz	6.25		500	Hz	2
Gyroscope Start-Up Time	Time from gyro enable to gyro drive ready		30		ms	3
Output Data Rate		12.5		1600	Hz	2

Table 1. Gyroscope Specifications

Notes:

1. Tested in production.
2. Guaranteed by design.
3. Derived from validation or characterization of parts, not tested in production.
4. Calculated from Rate Noise Spectral Density.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Conditions, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY						
Full-Scale Range	ACCEL_UI_FS_SEL=0		±16		*g*	2
	ACCEL_UI_FS_SEL=1		±8		*g*	2
	ACCEL_UI_FS_SEL=2		±4		*g*	2
	ACCEL_UI_FS_SEL=3		±2		*g*	2
ADC Word Length	Output in two's complement format		16		bits	2
Sensitivity Scale Factor	ACCEL_UI_FS_SEL=0		2,048		LSB/*g*	2
	ACCEL_UI_FS_SEL=1		4,096		LSB/*g*	2
	ACCEL_UI_FS_SEL=2		8,192		LSB/*g*	2
	ACCEL_UI_FS_SEL=3		16,384		LSB/*g*	2
Sensitivity Scale Factor Initial Tolerance	Component & Board-level, 25°C		±1		%	1
Sensitivity Change vs. Temperature	-40°C to +85°C		±0.01		%/°C	3
Nonlinearity	Best Fit Straight Line, ±2g		±0.2		%	3
Cross-Axis Sensitivity	Board-level		±2		%	3
ZERO-G OUTPUT						
Initial Tolerance	Board-level, all axes		±25		m*g*	3
Zero-G Level Change vs. Temperature	-40°C to +85°C		±0.25		m*g*/ºC	3
OTHER PARAMETERS						
Power Spectral Density	@ 10 Hz		110		µg/√Hz	3
RMS Noise	Bandwidth = 100 Hz		1.10		mg-rms	4
Low-Pass Filter Response		6.25		500	Hz	2
Accelerometer Startup Time	From sleep mode to valid data		10		ms	3
Output Data Rate		1.5625		1600	Hz	2

Table 2. Accelerometer Specifications

Notes:

1. Tested in production.
2. Guaranteed by design.
3. Derived from validation or characterization of parts, not tested in production.
4. Calculated from Power Spectral Density.

3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Conditions, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer		0.55		mA	2
	3-Axis Accelerometer		0.20		mA	2
	3-Axis Gyroscope		0.425		mA	2
Low-Power Mode	3-Axis Accelerometer, 25Hz ODR, 2x averaging		9.8		µA	2
	3-Axis Accelerometer, 100Hz ODR, 2x averaging		27.2		µA	2
Full-Chip Sleep Mode	At 25ºC		3.8		µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not tested in production.

3.3.2 A.C. Electrical Characteristics

Typical Operating Conditions, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Valid power-on RESET	0.1		100	ms	1
Power Supply Noise			10		mV peak-peak	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output	Output in two's complement format		0		LSB	3
ADC Resolution			16		bits	2
ODR	With Filter	1.5625		1600	Hz	2
Room Temperature Offset	25°C	-3		3	°C	3
Stabilization Time (fixed number of clock cycles)			77		µs	2
Sensitivity	Trimmed	125	126.9	129	LSB/°C	1
Sensitivity for FIFO data	Trimmed	1.95	1.983	2.01	LSB/°C	1
POWER-ON RESET						
Start-up time for register read/write	From power-up			1	ms	1
I²C ADDRESS						
I²C ADDRESS	AP_AD0 = 0 AP_AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			<10		pF	
DIGITAL OUTPUT (SDO, INT1, INT2)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1 MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1 MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	int_tpulse_duration= 0 , 1 (100us, 8us) ;	8		100	µs	
I²C I/O (SCL, SDA)						
V_{IL}, LOW-Level Input Voltage		-0.5 V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5 V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4 V V_{OL}=0.6 V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	CLKSEL=`2b00 or gyro inactive; 25°C	-3		+3	%	1
	CLK_SEL=`2b01 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=`2b00 or gyro inactive; -40°C to +85°C			±6.25	%	1
	CLK_SEL=`2b01 and gyro active; -40°C to +85°C			±1	%	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Expected results based on design, will be updated after characterization. Not tested in production.
2. Guaranteed by design.
3. To be Production tested.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Conditions, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE PLUS**					
f_{SCL}, SCL Clock Frequency				1	MHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		TBD			µs	1
t_{LOW}, SCL Low Period		TBD			µs	1
t_{HIGH}, SCL High Period		TBD			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		TBD			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		TBD			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		TBD			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400 pF			TBD	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400 pF			TBD	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		TBD			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		TBD			µs	1
C_b, Capacitive Load for each Bus Line			TBD		pF	1
$t_{VD.DAT}$, Data Valid Time				TBD	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				TBD	µs	1

Table 5. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

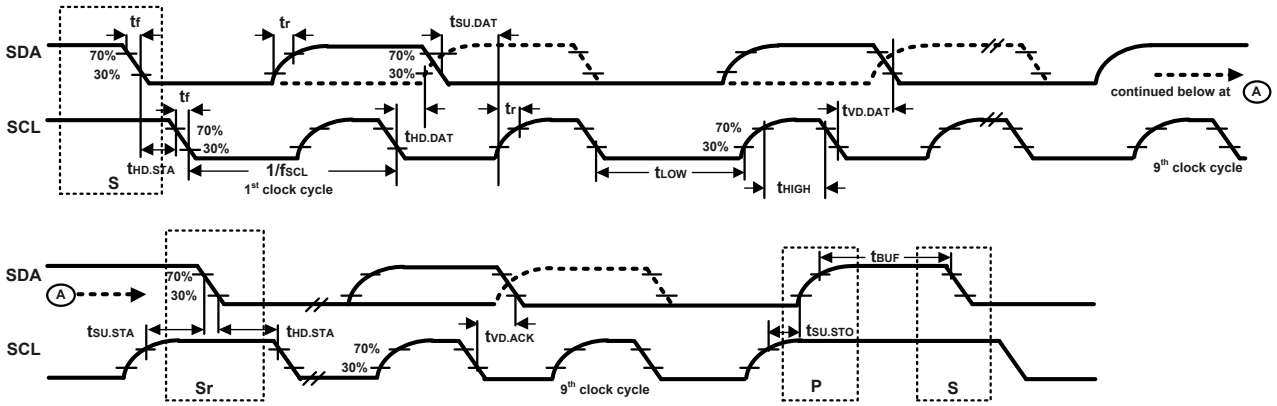

Figure 1. I²C Bus Timing Diagram

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3.5 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

Typical Operating Conditions, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			24	MHz	1
t_{LOW}, SCLK Low Period		TBD			ns	1
t_{HIGH}, SCLK High Period		TBD			ns	1
$t_{SU.CS}$, CS Setup Time		TBD			ns	1
$t_{HD.CS}$, CS Hold Time		TBD			ns	1
$t_{SU.SDI}$, SDI Setup Time		TBD			ns	1
$t_{HD.SDI}$, SDI Hold Time		TBD			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF			TBD	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20 pF	TBD			ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				TBD	ns	1

Table 6. 4-Wire SPI Timing Characteristics (24-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

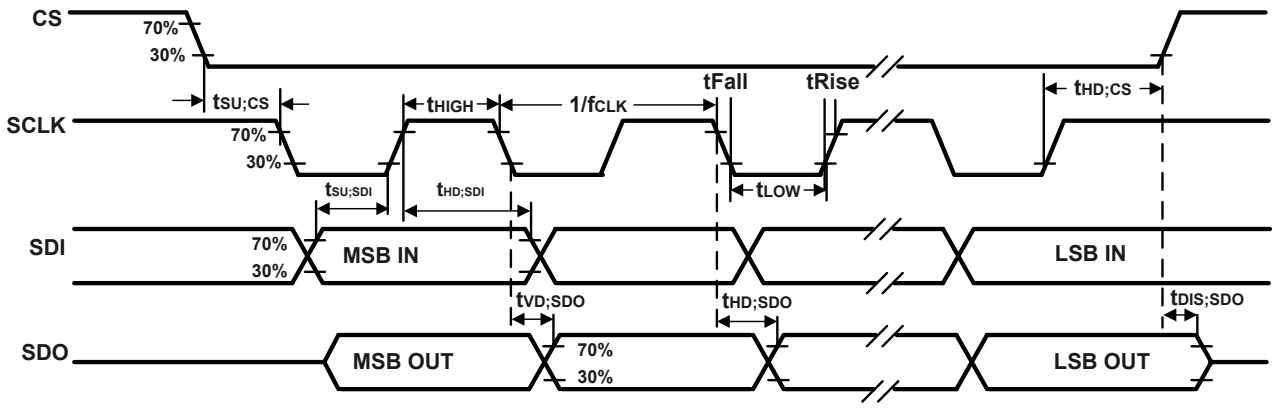

Figure 2. 4-Wire SPI Bus Timing Diagram

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3.6 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

Typical Operating Conditions, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			24	MHz	1
t_{LOW}, SCLK Low Period		TBD			ns	1
t_{HIGH}, SCLK High Period		TBD			ns	1
$t_{SU.CS}$, CS Setup Time		TBD			ns	1
$t_{HD.CS}$, CS Hold Time		TBD			ns	1
$t_{SU.SDIO}$, SDIO Input Setup Time		TBD			ns	1
$t_{HD.SDIO}$, SDIO Input Hold Time		TBD			ns	1
$t_{VD.SDIO}$, SDIO Output Valid Time	C_{load} = 20 pF			TBD	ns	1
$t_{HD.SDIO}$, SDIO Output Hold Time	C_{load} = 20 pF	TBD			ns	1
$t_{DIS.SDIO}$, SDIO Output Disable Time				TBD	ns	1

Table 7. 3-Wire SPI Timing Characteristics (24-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

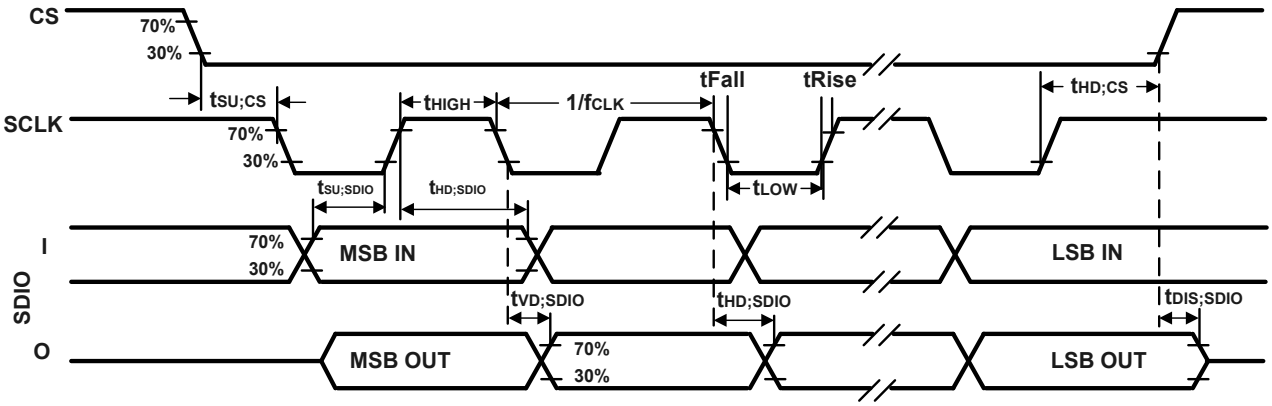

Figure 3. 3-Wire SPI Bus Timing Diagram

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3.7 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5 V to +4 V
Supply Voltage, VDDIO	-0.5 V to +4 V
Input Voltage Level (FSYNC, SCL, SDA)	-0.5 V to VDDIO + 0.5 V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 500 V (CDM)
Latch-up	JEDEC Class II (2),125°C ±100 mA

Table 8. Absolute Maximum Ratings

4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

Pin Number	Pin Name	Pin Description
1	AP_SDO / AP_AD0	AP_SDO: AP SPI serial data output (4-wire mode); AP_AD0: AP I3C^{SM} / I^{2}C slave address LSB
2	RESV	No Connect or Connect to GND or Connect to VDDIO
3	RESV	No Connect or Connect to GND or Connect to VDDIO
4	INT1 / INT	INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain) INT: All interrupts mapped to pin 4
5	VDDIO	IO power supply voltage
6	GND	Power supply ground
7	FSYNC	Frame sync input; Connect to GND if FSYNC not used
8	VDD	Power supply voltage
9	INT2	INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain)
10	RESV	No Connect or Connect to GND or Connect to VDDIO
11	RESV	No Connect or Connect to GND or Connect to VDDIO
12	AP_CS	AP SPI Chip select (AP SPI interface); Connect to VDDIO if using AP I3C^{SM} / I^{2}C interface
13	AP_SCL / AP_SCLK	AP_SCL: AP I3C^{SM} / I^{2}C serial clock; AP_SCLK: AP SPI serial clock
14	AP_SDA / AP_SDIO / AP_SDI	AP_SDA: AP I3C^{SM} / I^{2}C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode)

Table 9. Signal Descriptions

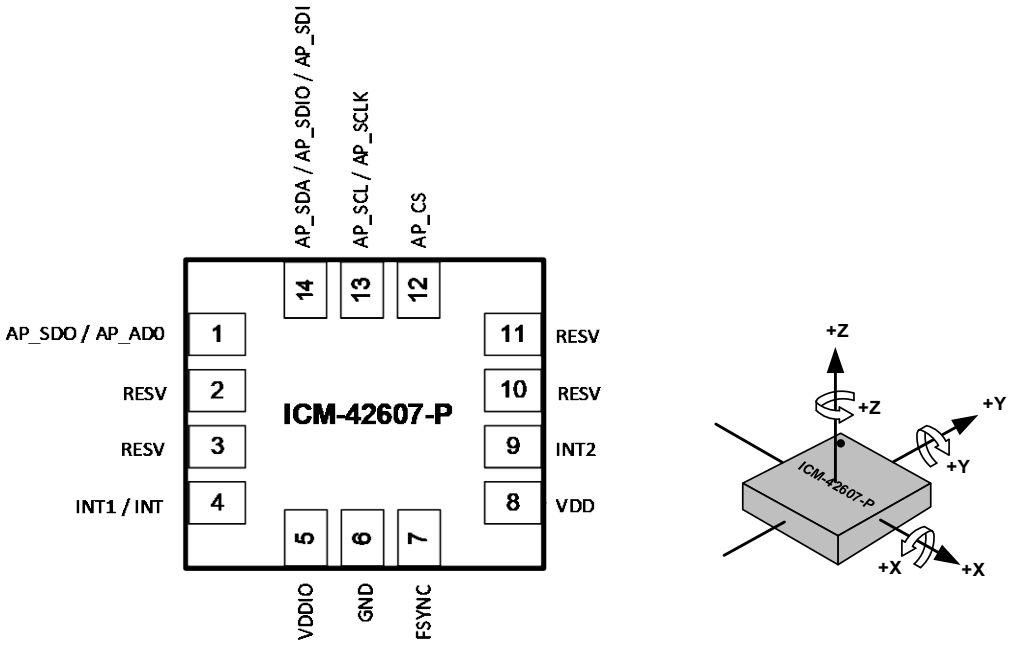

Figure 4. Pin Out Diagram for ICM-42607-P 2.5x3.0x0.76 mm LGA

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4.2 TYPICAL OPERATING CIRCUIT

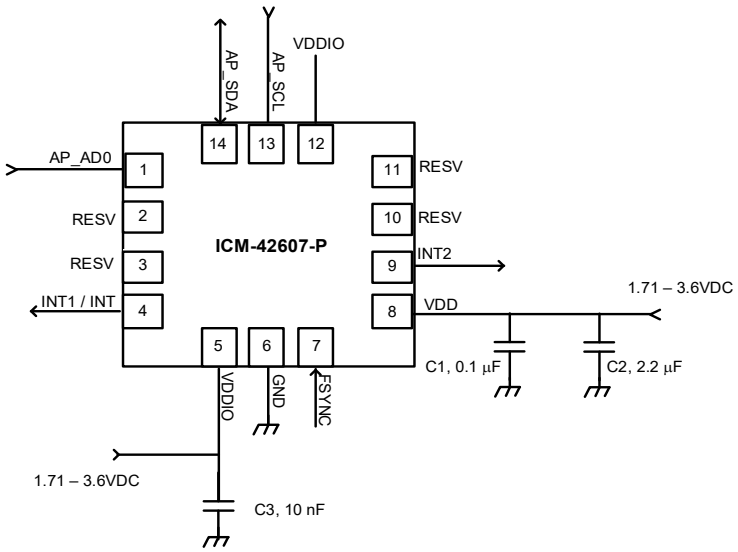

Figure 5. ICM-42607-P Application Schematic (I3C^{SM} / I^{2}C Interface to Host)

Note: I^{2}C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

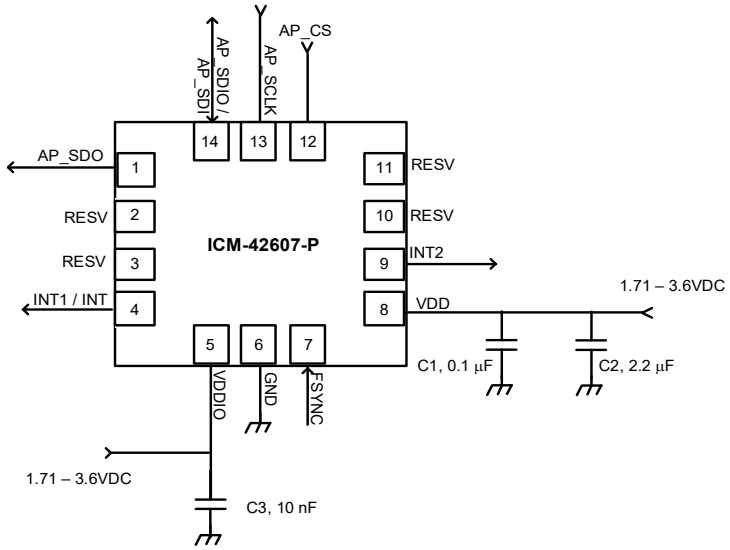

Figure 6. ICM-42607-P Application Schematic (SPI Interface to Host)

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4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

Component	Label	Specification	Quantity
VDD Bypass Capacitors	C1 C2	X7R, 0.1µF ±10% X7R, 2.2µF ±10%	1 1
VDDIO Bypass Capacitor	C3	X7R, 10nF ±10%	1

Table 10. Bill of Materials

4.4 SYSTEM BLOCK DIAGRAM

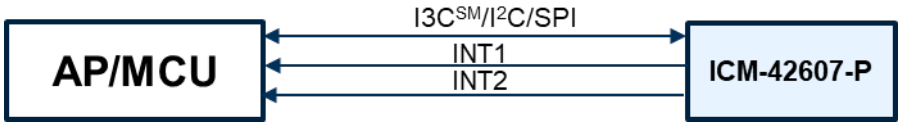

Figure 7. ICM-42607-P System Block Diagram

Note: The above block diagram is an example. Please refer to the pin-out (section 4.1) for other configuration options.

4.5 OVERVIEW

The ICM-42607-P is comprised of the following key blocks and functions:

- Three-axis MEMS gyroscope
- Three-axis MEMS accelerometer
- I3C^{SM}, I^{2}C and SPI serial communications interfaces to Host
- Self-Test
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE

The ICM-42607-P includes a vibratory MEMS rate gyroscope, which detects rotation about the X-, Y-, and Z- Axes. When the gyroscope is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using on-chip Analog-to-Digital Converter (ADC) to sample each axis. The full-scale range of the gyro sensor may be digitally programmed to ±250, ±500, ±1000, and ±2000 degrees per second (dps).

4.7 THREE-AXIS MEMS ACCELEROMETER

The ICM-42607-P includes a 3-Axis MEMS accelerometer. Acceleration along a particular axis induces displacement of a proof mass in the MEMS structure, and capacitive sensors detect the displacement. The ICM-42607-P architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. The full scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g* and ±16*g*.

4.8 I3C^{SM}, I^{2}C AND SPI HOST INTERFACE

The ICM-42607-P communicates to the application processor using an I3C^{SM}, I^{2}C, or SPI serial interface. The ICM-42607-P always acts as a slave when communicating to the application processor.

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers. When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response. The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

When the value of the self-test response is within the specified min/max limits, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.10 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers and are accessed via the serial interface. Data from these registers may be read any time.

4.11 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the interrupt pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) new data is available to be read (from the FIFO and Data registers); (2) accelerometer event interrupts; (3) FIFO watermark; (4) FIFO full. The interrupt status can be read from the Interrupt Status register.

4.12 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-42607-P die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.13 BIAS AND LDOS

The bias and LDO section generate the internal supply and the reference voltages and currents required by the ICM-42607-P.

4.14 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.15 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-42607-P.

Mode	Name	Gyro	Accel
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Low-Power Mode	Off	Duty-Cycled
4	Accelerometer Low-Noise Mode	Off	On
5	Gyroscope Low-Noise Mode	On	Off
6	6-Axis Low-Noise Mode	On	On

Table 11. Standard Power Modes for ICM-42607-P

5 PROGRAMMABLE INTERRUPTS

The ICM-42607-P has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. There are two interrupt outputs. Any interrupt may be mapped to either interrupt pin as explained in the register section. The following configuration options are available for the interrupts

- INT1 and INT2 can be push-pull or open drain
- Level or pulse mode
- Active high or active low

Additionally, ICM-42607-P includes In-band Interrupt (IBI) support for the I3C^{SM} interface.

6 DIGITAL INTERFACE

6.1 I3C^{SM}, I^{2}C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-42607-P can be accessed using I3C^{SM} at 12.5MHz (data rates up to 12.5Mbps in SDR mode, 25Mbps in DDR mode), I^{2}C at 1MHz or SPI at 24MHz. SPI operates in 3-wire or 4-wire mode. Pin assignments for serial interfaces are described in Section 4.1.

6.2 I3C^{SM} INTERFACE

I3C^{SM} is a new 2-wire digital interface comprised of the signals serial data (SDA) and serial clock (SCLK). I3C^{SM} is intended to improve upon the I^{2}C interface, while preserving backward compatibility.

I3C^{SM} carries the advantages of I^{2}C in simplicity, low pin count, easy board design, and multi-drop (vs. point to point), but provides the higher data rates, simpler pads, and lower power of SPI. I3C^{SM} adds higher throughput for a given frequency, in-band interrupts (from slave to master), dynamic addressing.

ICM-42607-P supports the following features of I3C^{SM}:

- SDR data rate up to 12.5Mbps
- DDR data rate up to 25Mbps
- Dynamic address allocation
- In-band Interrupt (IBI) support
- Support for asynchronous timing control mode 0
- Error detection (CRC and/or Parity)
- Common Command Code (CCC)

The ICM-42607-P always operates as an I3C^{SM} slave device when communicating to the system processor, which thus acts as the I3C^{SM} master. I3C^{SM} master controls an active pullup resistance on SDA, which it can enable and disable. The pullup resistance may be a board level resistor controlled by a pin, or it may be internal to the I3C^{SM} master.

6.3 I^{2}C INTERFACE

I^{2}C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^{2}C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-42607-P always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDDIO. The maximum bus speed is 1 MHz.

The slave address of the ICM-42607-P is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AP_AD0. This allows two ICM-42607-Ps to be connected to the same I^{2}C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AP_AD0 is logic low) and the address of the other should be b1101001 (pin AP_AD0 is logic high).

6.4 I^{2}C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I^{2}C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below). Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

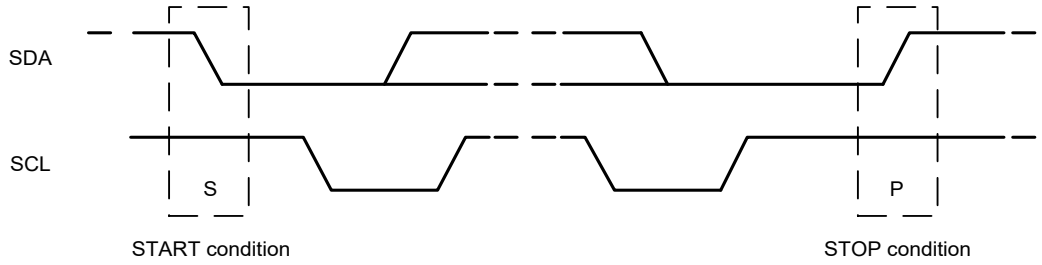

Figure 8. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready and releases the clock line (refer to the following figure).

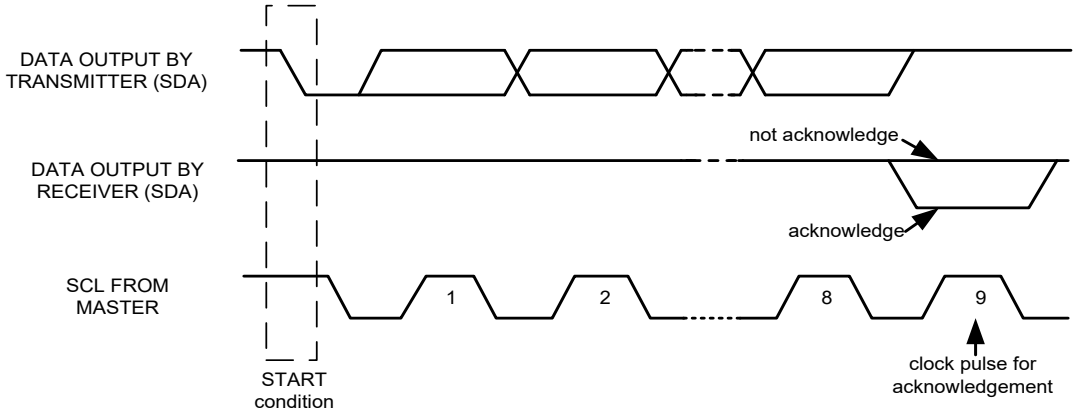

Figure 9. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

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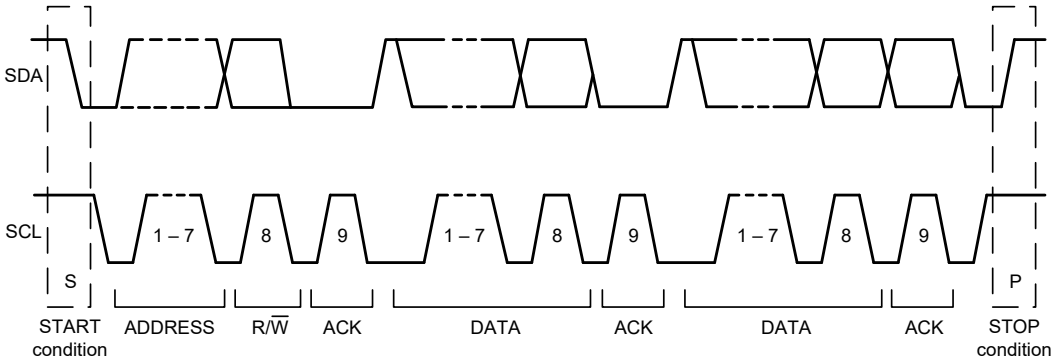

Figure 10. Complete I²C Data Transfer

To write the internal ICM-42607-P registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-42607-P acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-42607-P acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-42607-P automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-42607-P registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-42607-P, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-42607-P sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

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6.5 I²C TERMS

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ICM-42607-P internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 12. I²C Terms

6.6 SPI INTERFACE

The ICM-42607-P supports 3-wire or 4-wire SPI for the host interface. The ICM-42607-P always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO), the Serial Data Input (SDI), and the Serial Data IO (SDIO) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 24 MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Reads, data is two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

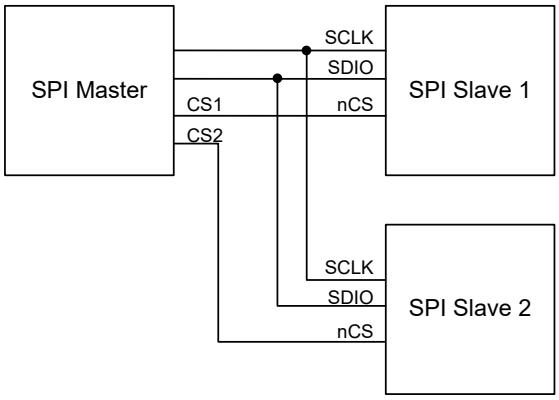

Figure 11. Typical SPI Master/Slave Configuration

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7 ASSEMBLY

This section provides general guidelines for assembling Micro Electro-Mechanical Systems (MEMS) devices packaged in LGA package.

7.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

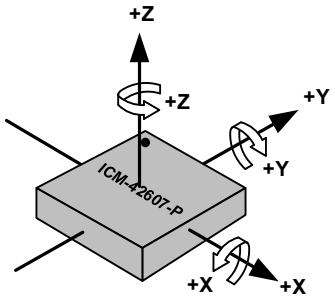

Figure 12. Orientation of Axes of Sensitivity and Polarity of Rotation

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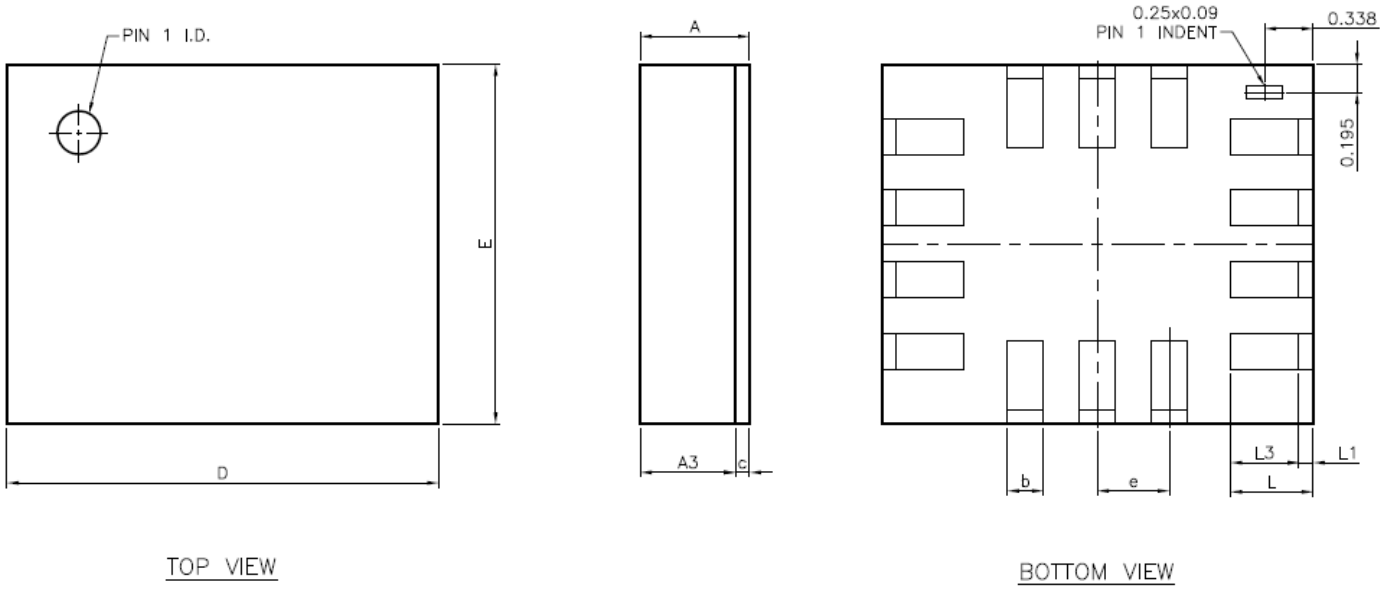
7.2 PACKAGE DIMENSIONS

14 Lead LGA (2.5x3x0.76) mm NiAu pad finish



TOP VIEW

BOTTOM VIEW

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.71	0.76	0.81
A3	---	0.65 REF.	---
b	0.20	0.25	0.30
c	---	0.1 REF.	---
D	2.95	3.00	3.05
E	2.45	2.50	2.55
e	---	0.50	---
L	0.525	0.575	0.625
L1	---	0.10	---
L3	0.425	0.475	0.525

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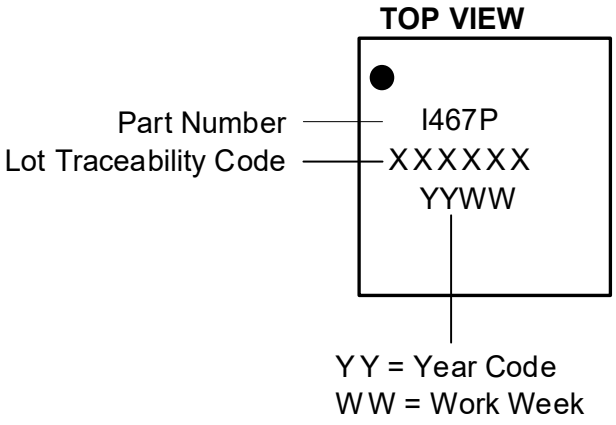
8 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-42607-P devices is summarized below:

Part Number	Part Number Package Marking
ICM-42607-P	I467P



9 REGISTER MAP

This section lists the register map for the ICM-42607-P, for user bank 0.

9.1 USER BANK 0 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01	01	DEVICE_CONFIG	R/W	-					SPI_AP_4WIRE	-	SPI_MODE
02	02	SIGNAL_PATH_RESET	R/W	-			SOFT_RESET_DEVICE_CONFIG	-	FIFO_FLUSH	-	
03	03	DRIVE_CONFIG1	R/W	-		I3C_DDR_SLEW_RATE			I3C_SDR_SLEW_RATE		
04	04	DRIVE_CONFIG2	R/W	-		I2C_SLEW_RATE			ALL_SLEW_RATE		
05	05	DRIVE_CONFIG3	R/W	-					SPI_SLEW_RATE		
06	06	INT_CONFIG	R/W	-		INT2_MODE	INT2_DRIVE_CIRCUIT	INT2_POLARITY	INT1_MODE	INT1_DRIVE_CIRCUIT	INT1_POLARITY
09	09	TEMP_DATA1	R	TEMP_DATA[15:8]							
0A	10	TEMP_DATA0	R	TEMP_DATA[7:0]							
0B	11	ACCEL_DATA_X1	R	ACCEL_DATA_X[15:8]							
0C	12	ACCEL_DATA_X0	R	ACCEL_DATA_X[7:0]							
0D	13	ACCEL_DATA_Y1	R	ACCEL_DATA_Y[15:8]							
0E	14	ACCEL_DATA_Y0	R	ACCEL_DATA_Y[7:0]							
0F	15	ACCEL_DATA_Z1	R	ACCEL _DATA_Z[15:8]							
10	16	ACCEL _DATA_Z0	R	ACCEL _DATA_Z[7:0]							
11	17	GYRO _DATA_X1	R	GYRO _DATA_X[15:8]							
12	18	GYRO _DATA_X0	R	GYRO _DATA_X[7:0]							
13	19	GYRO _DATA_Y1	R	GYRO_DATA_Y[15:8]							
14	20	GYRO _DATA_Y0	R	GYRO_DATA_Y[7:0]							
15	21	GYRO_DATA_Z1	R	GYRO_DATA_Z[15:8]							
16	22	GYRO_DATA_Z0	R	GYRO_DATA_Z[7:0]							
17	23	TMST_FSYNCH	R	TMST_FSYNC_DATA[15:8]							
18	24	TMST_FSYNCL	R	TMST_FSYNC_DATA[7:0]							
1D	29	APEX_DATA4	R	FF_DUR[7:0]							
1E	30	APEX_DATA5	R	FF_DUR[15:8]							
1F	31	PWR_MGMT0	R/W	ACCEL_LP_CLK_SEL	-		IDLE	GYRO_MODE		ACCEL_MODE	
20	32	GYRO_CONFIG0	R/W	-	GYRO_UI_FS_SEL		-	GYRO_ODR			
21	33	ACCEL_CONFIG0	R/W	-	ACCEL_UI_FS_SEL		-	ACCEL_ODR			
22	34	TEMP_CONFIG0	R/W	-	TEMP_FILT_BW			-			
23	35	GYRO_CONFIG1	R/W	-					GYRO_UI_FILT_BW		
24	36	ACCEL_CONFIG1	R/W	-	ACCEL_UI_AVG			-	ACCEL_UI_FILT_BW		
25	37	APEX_CONFIG0	R/W	-				DMP_POWER_SAVE_EN	DMP_INIT_EN	-	DMP_MEM_RESET_EN
26	38	APEX_CONFIG1	R/W	-	SMD_ENABLE	FF_ENABLE	TILT_ENABLE	PED_ENABLE	-	DMP_ODR	
27	39	WOM_CONFIG	R/W	-			WOM_INT_DUR		WOM_INT_MODE	WOM_MODE	WOM_EN
28	40	FIFO_CONFIG1	R/W	-						FIFO_MODE	FIFO_BYPASS
29	41	FIFO_CONFIG2	R/W	FIFO_WM[7:0]							
2A	42	FIFO_CONFIG3	R/W	-				FIFO_WM[11:8]			
2B	43	INT_SOURCE0	R/W	ST_INT1_EN	FSYNC_INT1_EN	PLL_RDY_INT1_EN	RESET_DONE_INT1_EN	DRDY_INT1_EN	FIFO_THS_INT1_EN	FIFO_FULL_INT1_EN	AGC_RDY_INT1_EN
2C	44	INT_SOURCE1	R/W	-	I3C_PROTOCOL_ERROR_INT1_EN	-		SMD_INT1_EN	WOM_Z_INT1_EN	WOM_Y_INT1_EN	WOM_X_INT1_EN
2D	45	INT_SOURCE3	R/W	ST_INT2_EN	FSYNC_INT2_EN	PLL_RDY_INT2_EN	RESET_DONE_INT2_EN	DRDY_INT2_EN	FIFO_THS_INT2_EN	FIFO_FULL_INT2_EN	AGC_RDY_INT2_EN

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Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2E	46	INT_SOURCE4	R/W	-	I3C_PROTOCOL_ERROR_INT2_EN	-		SMD_INT2_EN	WOM_Z_INT2_EN	WOM_Y_INT2_EN	WOM_X_INT2_EN
2F	47	FIFO_LOST_PKT0	R	FIFO_LOST_PKT_CNT[7:0]							
30	48	FIFO_LOST_PKT1	R	FIFO_LOST_PKT_CNT[15:8]							
31	49	APEX_DATA0	R	STEP_CNT[7:0]							
32	50	APEX_DATA1	R	STEP_CNT[15:8]							
33	51	APEX_DATA2	R	STEP_CADENCE							
34	52	APEX_DATA3	R	-					DMP_IDLE	ACTIVITY_CLASS	
35	53	INTF_CONFIG0	R/W	-	FIFO_COUNT_FORMAT	FIFO_COUNT_ENDIAN	SENSOR_DATA_ENDIAN	-		UI_SIFS_CFG	
36	54	INTF_CONFIG1	R/W	-				I3C_SDR_EN	I3C_DDR_EN	CLKSEL	
39	57	INT_STATUS_RDY	R/C	-							DATA_RDY_INT
3A	58	INT_STATUS	R/C	ST_INT	FSYNC_INT	PLL_RDY_INT	RESET_DONE_INT	-	FIFO_THS_INT	FIFO_FULL_INT	AGC_RDY_NT
3B	59	INT_STATUS2	R/C	-				SMD_INT	WOM_X_INT	WOM_Y_INT	WOM_Z_INT
3C	60	INT_STATUS3	R/C	-		STEP_DET_INT	STEP_CNT_OVF_INT	TILT_DET_INT	FF_DET_INT	-	
3D	61	FIFO_COUNTH	R	FIFO_COUNT[15:8]							
3E	62	FIFO_COUNTL	R	FIFO_COUNT[7:0]							
3F	63	FIFO_DATA	R	FIFO_DATA							
75	117	WHO_AM_I	R	WHOAMI							

Detailed register descriptions are provided in the sections that follow.

Register fields marked as Reserved must not be modified by the user. The Reset Value of the register can be used to determine the default value of reserved register fields, and unless otherwise noted this default value must be maintained even if the values of other register fields are modified by the user.

In the sections that follow, some register fields are described as can be changed on-the-fly even if sensor is on. These are the only register fields that can be changed on-the-fly even if sensor is on. Register fields not described as such must not be changed on-the-fly if sensor is on.

10 USER BANK 0 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 0.

Note: The device powers up in sleep mode.

10.1 DEVICE_CONFIG

Name: DEVICE_CONFIG
Address: 01 (01h)
Serial IF: R/W
Reset value: 0x04

BIT	NAME	FUNCTION
7:3	-	Reserved
2	SPI_AP_4WIRE	0: AP interface uses 3-wire SPI mode 1: AP interface uses 4-wire SPI mode
1	-	Reserved
0	SPI_MODE	SPI mode selection 0: Mode 0 and Mode 3 1: Mode 1 and Mode 2 If device is operating in non-SPI mode, user is not allowed to change the power-on default setting of this register. Change of this register setting will not take effect till AP_CS = 1.

10.2 SIGNAL_PATH_RESET

Name: SIGNAL_PATH_RESET
Address: 02 (02h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved
4	SOFT_RESET_DEVICE_CONFIG	Software Reset (auto clear bit) 0: Software reset not enabled 1: Software reset enabled
3	-	Reserved
2	FIFO_FLUSH	When set to 1, FIFO will get flushed. FIFO flush requires the following programming sequence: • Write FIFO_FLUSH =1 • Wait for 1.5µs • Read FIFO_FLUSH, it should now be 0 Host can only program this register bit to 1.
1:0	-	Reserved

10.3 DRIVE_CONFIG1

Name: DRIVE_CONFIG1 Address: 03 (03h) Serial IF: R/W Reset value: 0x2B		
BIT	**NAME**	**FUNCTION**
7:6	-	Reserved
5:3	I3C_DDR_SLEW_RATE	Controls slew rate for output pin 14 when device is in I3C^{SM} DDR protocol. While in I3C^{SM} operation, the device automatically switches to use I3C_DDR_SLEW_RATE after receiving ENTHDR0 ccc command from the host. The device automatically switches back to I3C_SDR_SLEW_RATE after the host issues HDR_EXIT pattern. 000: 20ns-60ns 001: 12ns-36ns 010: 6ns-18ns 011: 4ns-12ns 100: 2ns-6ns 101: < 2ns 110: Reserved 111: Reserved This register field should be programmed in I^{2}C or I3C/SDR mode, but not in I3C/DDR mode.
2:0	I3C_SDR_SLEW_RATE	Controls slew rate for output pin 14 in I3C^{SM} DDR protocol. After device reset, I2C_SLEW_RATE is used by default. If I3C^{SM} feature is enabled, the device automatically switches to use I3C_SDR_SLEW_RATE after receiving 0x7E+W message (an I3C^{SM} broadcast message). 000: 20ns-60ns 001: 12ns-36ns 010: 6ns-18ns 011: 4ns-12ns 100: 2ns-6ns 101: < 2ns 110: Reserved 111: Reserved This register should be programmed in I^{2}C or I3C/SDR mode, but not in I3C/DDR mode.

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10.4 DRIVE_CONFIG2

Name: DRIVE_CONFIG2 Address: 04 (04h) Serial IF: R/W Reset value: 0x0D		
BIT	**NAME**	**FUNCTION**
7:6	-	Reserved
5:3	I2C_SLEW_RATE	Controls slew rate for output pin 14 in I^2C mode. After device reset, the I2C_SLEW_RATE is used by default. If the 1st write operation from host is an SPI transaction, the device automatically switches to ALL_SLEW_RATE automatically. If $I3C^{SM}$ feature is enabled, the device automatically switches to I3C_SDR_SLEW_RATE after receiving 0x7E+W message (an I3C broadcast message). 000: 20ns-60ns 001: 12ns-36ns 010: 6ns-18ns 011: 4ns-12ns 100: 2ns-6ns 101: < 2ns 110: Reserved 111: Reserved This register field should be programmed in I^2C or I3C/SDR mode, but not in I3C/DDR mode.
2:0	ALL_SLEW_RATE	Configure drive strength for all output pins in all modes (SPI3, SPI4, I^2C, $I3C^{SM}$). This register also configures the drive strength of pin 14 when the device is in SPI mode. After device reset, the I2C_SLEW_RATE is used by default for pin 14. If the 1st write operation from the host is an SPI transaction, then the device switches to ALL_SLEW_RATE automatically. 000: 20ns-60ns 001: 12ns-36ns 010: 6ns-18ns 011: 4ns-12ns 100: 2ns-6ns 101: < 2ns 110: Reserved 111: Reserved This register should be programmed in I^2C or I3C/SDR mode, but not in I3C/DDR mode.

10.5 DRIVE_CONFIG3

Name: DRIVE_CONFIG3 Address: 05 (05h) Serial IF: R/W Reset value: 0x05		
BIT	**NAME**	**FUNCTION**
7:3	-	Reserved
2:0	SPI_SLEW_RATE	Controls slew rate for output pin 14 in SPI 3-wire or 4-wire mode After chip reset, the I2C_SLEW_RATE is used by default for pin 14 pin. If the 1st write operation from the host is an SPI3/4 transaction, the device automatically switches to SPI_SLEW_RATE. 000: 20ns-60ns 001: 12ns-36ns 010: 6ns-18ns 011: 4ns-12ns 100: 2ns-6ns 101: < 2ns 110: Reserved 111: Reserved This register field should be programmed in I^2C or I3C/SDR mode, but not in I3C/DDR mode.

10.6 INT_CONFIG

Name: INT_CONFIG Address: 06 (06h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:6	-	Reserved
5	INT2_MODE	INT2 interrupt mode 0: Pulsed mode 1: Latched mode
4	INT2_DRIVE_CIRCUIT	INT2 drive circuit 0: Open drain 1: Push pull
3	INT2_POLARITY	INT2 interrupt polarity 0: Active low 1: Active high
2	INT1_MODE	INT1 interrupt mode 0: Pulsed mode 1: Latched mode
1	INT1_DRIVE_CIRCUIT	INT1 drive circuit 0: Open drain 1: Push pull
0	INT1_POLARITY	INT1 interrupt polarity 0: Active low 1: Active high

10.7 TEMP_DATA1

Name: TEMP_DATA1 Address: 09 (09h) Serial IF: R Reset value: 0x80		
BIT	**NAME**	**FUNCTION**
7:0	TEMP_DATA[15:8]	Upper byte of temperature data

10.8 TEMP_DATA0

Name: TEMP_DATA0 Address: 10 (0Ah) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	TEMP_DATA[7:0]	Lower byte of temperature data

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

- Temperature in Degrees Centigrade = (TEMP_DATA / 128) + 25

Temperature data stored in FIFO can be an 8-bit or 16-bit quantity, depending on packet format. It can be converted to degrees centigrade by using the following formulas:

- 8-bit quantity: Temperature in Degrees Centigrade = (TEMP_DATA / 2) + 25; where TEMP_DATA refers to the 8 MSBs of the 16-bit word coming from the temperature sensor. In this mode the 8 LSBs are set to '0'.

- 16-bit quantity: Temperature in Degrees Centigrade = (TEMP_DATA / 128) + 25

10.9 ACCEL_DATA_X1

Name: ACCEL_DATA_X1 Address: 11 (0Bh) Serial IF: R Reset value: 0x80		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_DATA_X[15:8]	Upper byte of Accel X-axis data

10.10 ACCEL_DATA_X0

Name: ACCEL_DATA_X0 Address: 12 (0Ch) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_DATA_X[7:0]	Lower byte of Accel X-axis data

10.11 ACCEL_DATA_Y1

Name: ACCEL_DATA_Y1
Address: 13 (0Dh)
Serial IF: R
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y[15:8]	Upper byte of Accel Y-axis data

10.12 ACCEL_DATA_Y0

Name: ACCEL_DATA_Y0
Address: 14 (0Eh)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y[7:0]	Lower byte of Accel Y-axis data

10.13 ACCEL_DATA_Z1

Name: ACCEL_DATA_Z1
Address: 15 (0Fh)
Serial IF: R
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z[15:8]	Upper byte of Accel Z-axis data

10.14 ACCEL_DATA_Z0

Name: ACCEL_DATA_Z0
Address: 16 (10h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z[7:0]	Lower byte of Accel Z-axis data

10.15 GYRO_DATA_X1

Name: GYRO_DATA_X1
Address: 17 (11h)
Serial IF: R
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	GYRO_DATA_X[15:8]	Upper byte of Gyro X-axis data

10.16 GYRO_DATA_X0

Name: GYRO_DATA_X0 Address: 18 (12h) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_X[7:0]	Lower byte of Gyro X-axis data

10.17 GYRO_DATA_Y1

Name: GYRO_DATA_Y1 Address: 19 (13h) Serial IF: R Reset value: 0x80		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_Y[15:8]	Upper byte of Gyro Y-axis data

10.18 GYRO_DATA_Y0

Name: GYRO_DATA_Y0 Address: 20 (14h) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_Y[7:0]	Lower byte of Gyro Y-axis data

10.19 GYRO_DATA_Z1

Name: GYRO_DATA_Z1 Address: 21 (15h) Serial IF: R Reset value: 0x80		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_Z[15:8]	Upper byte of Gyro Z-axis data

10.20 GYRO_DATA_Z0

Name: GYRO_DATA_Z0 Address: 22 (16h) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	GYRO_DATA_Z[7:0]	Lower byte of Gyro Z-axis data

10.21 TMST_FSYNCH

Name: TMST_FSYNCH Address: 23 (17h) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	TMST_FSYNC_DATA[15:8]	Stores the upper byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

10.22 TMST_FSYNCL

Name: TMST_FSYNCL Address: 24 (18h) Serial IF: SYNCR Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	TMST_FSYNC_DATA[7:0]	Stores the lower byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

10.23 APEX_DATA4

Name: APEX_DATA4 Address: 29 (1Dh) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	FF_DUR[7:0]	Lower byte of Freefall Duration The duration is given in number of samples and it can be converted to freefall distance in meters by applying the following formula: FF_DISTANCE = 0.5*9.81*(FF_DUR*DMP_ODR_S)^2 Note: DMP_ODR_D is the duration of DMP_ODR expressed in seconds.

10.24 APEX_DATA5

Name: APEX_DATA5 Address: 30 (1Eh) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	FF_DUR[15:8]	Upper byte of Freefall Duration The duration is given in number of samples and it can be converted to freefall distance in meters by applying the following formula: FF_DISTANCE = 0.5*9.81*(FF_DUR*DMP_ODR_S)^2 Note: DMP_ODR_D is the duration of DMP_ODR expressed in seconds.

10.25 PWR_MGMT0

Name: PWR_MGMT0 Address: 31 (1Fh) Serial IF: R/W Reset value: 0x80		
BIT	**NAME**	**FUNCTION**
7	ACCEL_LP_CLK_SEL	0: Accelerometer LP mode uses Wake Up oscillator clock 1: Accelerometer LP mode uses RC oscillator clock This field can be changed on-the-fly even if accel sensor is on
6:5	-	Reserved
4	IDLE	If this bit is set to 1, the RC oscillator is powered on even if Accel and Gyro are powered off. Nominally this bit is set to 0, so when Accel and Gyro are powered off, the chip will go to OFF state, since the RC oscillator will also be powered off This field can be changed on-the-fly even if a sensor is on
3:2	GYRO_MODE	00: Turns gyroscope off 01: Places gyroscope in Standby Mode 10: Reserved 11: Places gyroscope in Low Noise (LN) Mode Gyroscope needs to be kept ON for a minimum of 45ms. When transitioning from OFF to any of the other modes, do not issue any register writes for 200µs. This field can be changed on-the-fly even if gyro sensor is on
1:0	ACCEL_MODE	00: Turns accelerometer off (default) 01: Turns accelerometer off 10: Places accelerometer in Low Power (LP) Mode 11: Places accelerometer in Low Noise (LN) Mode When transitioning from OFF to any of the other modes, do not issue any register writes for 200µs. This field can be changed on-the-fly even if accel sensor is on

10.26 GYRO_CONFIG0

Name: GYRO_CONFIG0 Address: 32 (20h) Serial IF: R/W Reset value: 0x06		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6:5	GYRO_UI_FS_SEL	Full scale select for gyroscope UI interface output 000: ±2000dps 001: ±1000dps 010: ±500dps 011: ±250dps This field can be changed on-the-fly even if gyro sensor is on
4	-	Reserved
3:0	GYRO_ODR	Gyroscope ODR selection for UI interface output 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 1.6kHz 0110: 800Hz 0111: 400Hz 1000: 200Hz 1001: 100Hz 1010: 50Hz 1011: 25Hz 1100: 12.5Hz 1101: Reserved 1110: Reserved 1111: Reserved This field can be changed on-the-fly even if gyro sensor is on

10.27 ACCEL_CONFIG0

Name: ACCEL_CONFIG0 Address: 33 (21h) Serial IF: R/W Reset value: 0x06		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6:5	ACCEL_UI_FS_SEL	Full scale select for accelerometer UI interface output 000: ±16g 001: ±8g 010: ±4g 011: ±2g This field can be changed on-the-fly even if accel sensor is on
4	-	Reserved
3:0	ACCEL_ODR	Accelerometer ODR selection for UI interface output 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 1.6kHz (LN mode) 0110: 800Hz (LN mode) 0111: 400Hz (LP or LN mode) 1000: 200Hz (LP or LN mode) 1001: 100Hz (LP or LN mode) 1010: 50Hz (LP or LN mode) 1011: 25Hz (LP or LN mode) 1100: 12.5Hz (LP or LN mode) 1101: 6.25Hz (LP mode) 1110: 3.125Hz (LP mode) 1111: 1.5625Hz (LP mode) This field can be changed on-the-fly when accel sensor is on

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10.28 TEMP_CONFIG0

Name: TEMP_CONFIG0 Address: 34 (22h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6:4	TEMP_FILT_BW	Sets the bandwidth of the temperature signal DLPF 000: DLPF bypassed 001: DLPF BW = 180Hz 010: DLPF BW = 72Hz 011: DLPF BW = 34Hz 100: DLPF BW = 16Hz 101: DLPF BW = 8Hz 110: DLPF BW = 4Hz 111: DLPF BW = 4Hz This field can be changed on-the-fly even if sensor is on
3:0	-	Reserved

10.29 GYRO_CONFIG1

Name: GYRO_CONFIG1 Address: 35 (23h) Serial IF: R/W Reset value: 0x31		
BIT	**NAME**	**FUNCTION**
7:3	-	Reserved
2:0	GYRO_UI_FILT_BW	Selects GYRO UI low pass filter bandwidth 000: Low pass filter bypassed 001: 180Hz 010: 121Hz 011: 73Hz 100: 53Hz 101: 34Hz 110: 25Hz 111: 16Hz This field can be changed on-the-fly even if gyro sensor is on

10.30 ACCEL_CONFIG1

Name: ACCEL_CONFIG1 Address: 36 (24h) Serial IF: R/W Reset value: 0x31		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6:4	ACCEL_UI_AVG	Selects averaging filter setting to create accelerometer output in accelerometer low power mode (LPM) 000: 2x average 001: 4x average 010: 8x average 011: 16x average 100: 32x average 101: 64x average 110: 64x average 111: 64x average This field cannot be changed when the accel sensor is in LPM
3	-	Reserved
2:0	ACCEL_UI_FILT_BW	Selects ACCEL UI low pass filter bandwidth 000: Low pass filter bypassed 001: 180Hz 010: 121Hz 011: 73Hz 100: 53Hz 101: 34Hz 110: 25Hz 111: 16Hz This field can be changed on-the-fly even if accel sensor is on

10.31 APEX_CONFIG0

Name: APEX_CONFIG0 Address: 37 (25h) Serial IF: R/W Reset value: 0x08		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3	DMP_POWER_SAVE_EN	When this bit is set to 1, power saving is enabled for DMP algorithms
2	DMP_INIT_EN	When this bit is set to 1, the DMP is enabled This field can be changed on-the-fly even if accel sensor is on
1	-	Reserved
0	DMP_MEM_RESET_EN	When this bit is set to 1, it clears DMP SRAM for APEX operation or Self-test operation.

10.32 APEX_CONFIG1

Name: APEX_CONFIG1 Address: 38 (26h) Serial IF: R/W Reset value: 0x02		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6	SMD_ENABLE	0: Significant Motion Detection not enabled 1: Significant Motion Detection enabled This field can be changed on-the-fly even if accel sensor is on
5	FF_ENABLE	0: Freefall Detection not enabled 1: Freefall Detection enabled This field can be changed on-the-fly even if accel sensor is on
4	TILT_ENABLE	0: Tilt Detection not enabled 1: Tilt Detection enabled This field can be changed on-the-fly even if accel sensor is on
3	PED_ENABLE	0: Pedometer not enabled 1: Pedometer enabled This field can be changed on-the-fly even if accel sensor is on
2	-	Reserved
1:0	DMP_ODR	00: 25Hz 01: 400Hz 10: 50Hz 11: 100Hz The ACCEL_ODR field must be configured to an ODR equal or greater to the DMP_ODR field, for correct device operation. This field can be changed on-the-fly even if accel sensor is on

10.33 WOM_CONFIG

Name: WOM_CONFIG Address: 39 (27h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:5	-	Reserved
4:3	WOM_INT_DUR	Selects Wake on Motion interrupt assertion from among the following options 00: Reserved 01: WoM interrupt asserted at second overthreshold event 10: WoM interrupt asserted at third overthreshold event 11: WoM interrupt asserted at fourth overthreshold event This field can be changed on-the-fly even if accel sensor is on, but it cannot be changed if WOM_EN is already enabled
2	WOM_INT_MODE	0: Set WoM interrupt on the OR of all enabled accelerometer thresholds 1: Set WoM interrupt on the AND of all enabled accelerometer thresholds This field can be changed on-the-fly even if accel sensor is on, but it cannot be changed if WOM_EN is already enabled
1	WOM_MODE	0: Initial sample is stored. Future samples are compared to initial sample 1: Compare current sample to previous sample This field can be changed on-the-fly even if accel sensor is on, but it cannot be changed if WOM_EN is already enabled
0	WOM_EN	0: WOM disabled 01: WOM enabled This field can be changed on-the-fly even if accel sensor is on

10.34 FIFO_CONFIG1

Name: FIFO_CONFIG1 Address: 40 (28h) Serial IF: R/W Reset value: 0x01		
BIT	**NAME**	**FUNCTION**
7:2	-	Reserved
1	FIFO_MODE	FIFO mode control 0: Stream-to-FIFO Mode 1: STOP-on-FULL Mode
0	FIFO_BYPASS	FIFO bypass control 0: FIFO is not bypassed 1: FIFO is bypassed

10.35 FIFO_CONFIG2

Name: FIFO_CONFIG2 Address: 41 (29h) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_WM[7:0]	Lower bits of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes or records according to FIFO_COUNT_FORMAT setting. FIFO_WM_EN must be zero before writing this register. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source. This field should be changed when FIFO is empty to avoid spurious interrupts.

10.36 FIFO_CONFIG3

Name: FIFO_CONFIG3 Address: 42 (2Ah) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3:0	FIFO_WM[11:8]	Upper bits of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes or records according to FIFO_COUNT_FORMAT setting. FIFO_WM_EN must be zero before writing this register. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source. This field should be changed when FIFO is empty to avoid spurious interrupts.

10.37 INT_SOURCE0

Name: INT_SOURCE0 Address: 43 (2Bh) Serial IF: R/W Reset value: 0x10		
BIT	**NAME**	**FUNCTION**
7	ST_INT1_EN	0: Self-Test Done interrupt not routed to INT1 1: Self-Test Done interrupt routed to INT1
6	FSYNC_INT1_EN	0: FSYNC interrupt not routed to INT1 1: FSYNC interrupt routed to INT1
5	PLL_RDY_INT1_EN	0: PLL ready interrupt not routed to INT1 1: PLL ready interrupt routed to INT1
4	RESET_DONE_INT1_EN	0: Reset done interrupt not routed to INT1 1: Reset done interrupt routed to INT1
3	DRDY_INT1_EN	0: Data Ready interrupt not routed to INT1 1: Data Ready interrupt routed to INT1
2	FIFO_THS_INT1_EN	0: FIFO threshold interrupt not routed to INT1 1: FIFO threshold interrupt routed to INT1
1	FIFO_FULL_INT1_EN	0: FIFO full interrupt not routed to INT1 1: FIFO full interrupt routed to INT1 To avoid FIFO FULL interrupts while reading FIFO, this bit should be disabled while reading FIFO
0	AGC_RDY_INT1_EN	0: UI AGC ready interrupt not routed to INT1 1: UI AGC ready interrupt routed to INT1

10.38 INT_SOURCE1

Name: INT_SOURCE1 Address: 44 (2Ch) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6	I3C_PROTOCOL_ERROR_INT1_EN	0: I3C^{SM} protocol error interrupt not routed to INT1 1: I3C^{SM} protocol error interrupt routed to INT1
5:4	-	Reserved
3	SMD_INT1_EN	0: SMD interrupt not routed to INT1 1: SMD interrupt routed to INT1
2	WOM_Z_INT1_EN	0: Z-axis WOM interrupt not routed to INT1 1: Z-axis WOM interrupt routed to INT1
1	WOM_Y_INT1_EN	0: Y-axis WOM interrupt not routed to INT1 1: Y-axis WOM interrupt routed to INT1
0	WOM_X_INT1_EN	0: X-axis WOM interrupt not routed to INT1 1: X-axis WOM interrupt routed to INT1

10.39 INT_SOURCE3

Name: INT_SOURCE3 Address: 45 (2Dh) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7	ST_INT2_EN	0: Self-Test Done interrupt not routed to INT2 1: Self-Test Done interrupt routed to INT2
6	FSYNC_INT2_EN	0: FSYNC interrupt not routed to INT2 1: FSYNC interrupt routed to INT2
5	PLL_RDY_INT2_EN	0: PLL ready interrupt not routed to INT2 1: PLL ready interrupt routed to INT2
4	RESET_DONE_INT2_EN	0: Reset done interrupt not routed to INT2 1: Reset done interrupt routed to INT2
3	DRDY_INT2_EN	0: Data Ready interrupt not routed to INT2 1: Data Ready interrupt routed to INT2
2	FIFO_THS_INT2_EN	0: FIFO threshold interrupt not routed to INT2 1: FIFO threshold interrupt routed to INT2
1	FIFO_FULL_INT2_EN	0: FIFO full interrupt not routed to INT2 1: FIFO full interrupt routed to INT2
0	AGC_RDY_INT2_EN	0: AGC ready interrupt not routed to INT2 1: AGC ready interrupt routed to INT2

10.40 INT_SOURCE4

Name: INT_SOURCE4 Address: 46 (2Eh) Serial IF: R/W Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6	I3C_PROTOCOL_ERROR_INT2_EN	0: I3C^{SM} protocol error interrupt not routed to INT2 1: I3C^{SM} protocol error interrupt routed to INT2
5:4	-	Reserved
3	SMD_INT2_EN	0: SMD interrupt not routed to INT2 1: SMD interrupt routed to INT2
2	WOM_Z_INT2_EN	0: Z-axis WOM interrupt not routed to INT2 1: Z-axis WOM interrupt routed to INT2
1	WOM_Y_INT2_EN	0: Y-axis WOM interrupt not routed to INT2 1: Y-axis WOM interrupt routed to INT2
0	WOM_X_INT2_EN	0: X-axis WOM interrupt not routed to INT2 1: X-axis WOM interrupt routed to INT2

10.41 FIFO_LOST_PKT0

Name: FIFO_LOST_PKT0
Address: 47 (2Fh)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_LOST_PKT_CNT[7:0]	Low byte, number of packets lost in the FIFO

10.42 FIFO_LOST_PKT1

Name: FIFO_LOST_PKT1
Address: 48 (30h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_LOST_PKT_CNT[15:8]	High byte, number of packets lost in the FIFO

10.43 APEX_DATA0

Name: APEX_DATA0
Address: 49 (31h)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	STEP_CNT[7:0]	Pedometer Output: Lower byte of Step Count measured by pedometer

10.44 APEX_DATA1

Name: APEX_DATA1
Address: 50 (32h)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	STEP_CNT[15:8]	Pedometer Output: Upper byte of Step Count measured by pedometer

10.45 APEX_DATA2

Name: APEX_DATA2
Address: 51 (33h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	STEP_CADENCE	Pedometer Output: Walk/run cadency in number of samples. Format is u6.2. e.g. At 50Hz ODR and 2Hz walk frequency, the cadency is 25 samples and the register will output 100.

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10.46 APEX_DATA3

Name: APEX_DATA3 Address: 52 (34h) Serial IF: R Reset value: 0x04		
BIT	**NAME**	**FUNCTION**
7:3	-	Reserved
2	DMP_IDLE	0: Indicates DMP is running 1: Indicates DMP is idle
1:0	ACTIVITY_CLASS	Pedometer Output: Detected activity 00: Unknown 01: Walk 10: Run 11: Reserved

10.47 INTF_CONFIG0

Name: INTF_CONFIG0 Address: 53 (35h) Serial IF: R/W Reset value: 0x30		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6	FIFO_COUNT_FORMAT	0: FIFO count is reported in bytes 1: FIFO count is reported in records (1 record = 16 bytes for header + gyro + accel + temp sensor data + time stamp, or 8 bytes for header + gyro/accel + temp sensor data)
5	FIFO_COUNT_ENDIAN	This bit applies to FIFO Count and Lost Packet Count 0: Reported in Little Endian format 1: Reported in Big Endian format
4	SENSOR_DATA_ENDIAN	0: Sensor data is reported in Little Endian format 1: Sensor data is reported in Big Endian format
3:2	-	Reserved
1:0	UI_SIFS_CFG	0x: Reserved 10: Disable SPI 11: Disable I^2C

10.48 INTF_CONFIG1

Name: INTF_CONFIG1 Address: 54 (36h) Serial IF: R/W Reset value: 0x4C		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3	I3C_SDR_EN	0: I3C^{SM} SDR mode not enabled 1: I3C^{SM} SDR mode enabled Device will be in pure I^{2}C mode if {I3C_SDR_EN, I3C_DDR_EN} = 00
2	I3C_DDR_EN	0: I3C^{SM} DDR mode not enabled 1: I3C^{SM} DDR mode enabled This bit will not take effect unless I3C_SDR_EN = 1.
1:0	CLKSEL	00: Always select internal RC oscillator 01: Select PLL when available, else select RC oscillator (default) 10: Reserved 11: Disable all clocks

10.49 INT_STATUS_DRDY

Name: INT_STATUS_DRDY Address: 57 (39h) Serial IF: R/C Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:1	-	Reserved
0	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.

10.50 INT_STATUS

Name: INT_STATUS
Address: 58 (3Ah)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7	ST_INT	This bit automatically sets to 1 when a Self Test done interrupt is generated. The bit clears to 0 after the register has been read.
6	FSYNC_INT	This bit automatically sets to 1 when an FSYNC interrupt is generated. The bit clears to 0 after the register has been read.
5	PLL_RDY_INT	This bit automatically sets to 1 when a PLL Ready interrupt is generated. The bit clears to 0 after the register has been read.
4	RESET_DONE_INT	This bit automatically sets to 1 when software reset is complete. The bit clears to 0 after the register has been read.
3	-	Reserved
2	FIFO_THS_INT	This bit automatically sets to 1 when the FIFO buffer reaches the threshold value. The bit clears to 0 after the register has been read.
1	FIFO_FULL_INT	This bit automatically sets to 1 when the FIFO buffer is full. The bit clears to 0 after the register has been read.
0	AGC_RDY_INT	This bit automatically sets to 1 when an AGC Ready interrupt is generated. The bit clears to 0 after the register has been read.

10.51 INT_STATUS2

Name: INT_STATUS2
Address: 59 (3Bh)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3	SMD_INT	Significant Motion Detection Interrupt, clears on read
2	WOM_X_INT	Wake on Motion Interrupt on X-axis, clears on read
1	WOM_Y_INT	Wake on Motion Interrupt on Y-axis, clears on read
0	WOM_Z_INT	Wake on Motion Interrupt on Z-axis, clears on read

10.52 INT_STATUS3

Name: INT_STATUS3
Address: 60 (3Ch)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	STEP_DET_INT	Step Detection Interrupt, clears on read
4	STEP_CNT_OVF_INT	Step Count Overflow Interrupt, clears on read
3	TILT_DET_INT	Tilt Detection Interrupt, clears on read
2	FF_DET_INT	Freefall Interrupt, clears on read
1:0	-	Reserved

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10.53 FIFO_COUNTH

Name: FIFO_COUNTH Address: 61 (3Dh) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_COUNT[15:8]	High Bits, count indicates the number of records or bytes available in FIFO according to FIFO_COUNT_FORMAT setting. Note: Must read FIFO_COUNTL to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

10.54 FIFO_COUNTL

Name: FIFO_COUNTL Address: 62 (3Eh) Serial IF: R Reset value: 0x00		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_COUNT[7:0]	Low Bits, count indicates the number of records or bytes available in FIFO according to FIFO_COUNT_REC setting. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

10.55 FIFO_DATA

Name: FIFO_DATA Address: 63 (3Fh) Serial IF: R Reset value: 0xFF		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_DATA	FIFO data port

10.56 WHO_AM_I

Name: WHO_AM_I Address: 117 (75h) Serial IF: R Reset value: 0x60		
BIT	**NAME**	**FUNCTION**
7:0	WHOAMI	Register to indicate to user which device is being accessed

Description:

This register is used to verify the identity of the device. The contents of WHOAMI is an 8-bit device ID. The default value of the register is 0x60. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor.

11 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

12 DOCUMENT INFORMATION

12.1 REVISION HISTORY

Revision Date	Revision	Description
10/20/2020	0.1	Initial Release

InvenSense